REMARKS

Claims 1-17 are pending in the present application. Claims 1 and 2 are allowed. Claims 3 to 17 are rejected. The Examiner's reconsideration of the rejection is respectfully requested in view of the above amendment and the following remarks.

The drawings were objected to for failure to include numeral "100" as described in the specification. Proposed corrected Figure 1 with the numeral "100" inserted is submitted for the Examiner's approval. As to the Examiner's objection to failure of inclusion of the label "COPI", applicant respectfully submits that in each reference to the label COPI in the specification, it is followed by numeral "116", which is clearly shown in the drawings. Thus, there is no confusion as to which signal line is COPI. Thus, insertion of the label "COPI" in the drawings is not believed to be necessary. Approval of the corrected drawing by the Examiner is respectfully requested.

In paragraph two of the office action, it is indicated that "Figure 5 is not mention and described in the section of "Detailed Description of Preferred Embodiment of the Invention" in the specification".

The Examiner's attention is respectfully directed to page 9, line 22, which states, inter alia "Figure 5 illustrates the distribution of the instruction bits according to an embodiment of the present invention." Withdrawal of the objection is respectfully requested.

Applicant gratefully acknowledges the Examiner's indication that claims 1 and 2 are allowed.

Claims 3 to 17 were rejected under 35 U.S.C. 112, first paragraph. The Examiner states, "in claim 3, "the main processor instructions are m-bits and the coprocessor instructions are m+n

bits, the n bits being stored in the coprocessor program memory" was not described in the specification. In claim 4, "said m-bits of said main processor instruction are fetched from the main program memory by the main processor and sent to the coprocessor" was not described in the specification. Note only (m-c) bits are sent to the coprocessor. Similar problems exist in the other claims 6 and 8."

Claim 3 has been amended to remove the specification of the actual lengths of the main processor instruction and the coprocessor instruction. Thus, the rejection of claim 3 under 112, first paragraph is rendered moot.

With respect to the rejection of claims 4, 6, and 8 under 35 U.S.C. 112, first paragraph, applicant respectfully traverses. Although the specification describes an exemplary embodiment which describes, the exemplary feature of forwarding (m-c) bits from the main processor to the coprocessor (see for example, pages 9 and 10 of the specification), the specification describes other embodiments which, for example, places the predecoder within the coprocessor (see page 13, line 20 to page 14, line 3). In such configuration, one skilled in the art reviewing the description in the specification and the drawings as shown, for example, in figure 1, would readily appreciate that the entire m-bit instruction (including the 'c' bits) accessed from main program memory would be sent to the coprocessor, facilitating a predecoding function performed within the coprocessor. Claims 4 to 8 as originally submitted are therefore supported by the description of such configuration to enable one skilled in the art to make the invention as claimed.

With respect to the feature described in pages 9 and 10 of the specification, namely, forwarding the (m-c)-bit instruction to the coprocessor, new claims 18 and 19 are added to

further define such embodiment.

With respect to claim 9, the Examiner indicated that "a common program address used by both the main processor and coprocessor" was not described in the specification.

The Examiner's attention is respectfully directed to page 7, line 21 wherein it is stated, "An address, preferably 16 bits, is sent via address bus 130 to main program memory 140 and coprocessor program memory (CPM) 160. MPM 140 and CPM 160 output the addressed instruction onto Main Program Bus...". Applicant respectfully submits that the above passage clearly shows that instructions for the main processor and coprocessor are accessed using a 'common program address', essentially as claimed in claim 9. The Examiner's reconsideration of rejection is respectfully requested.

For the foregoing reasons, it is believed that claims 3 to 17 satisfy the requirements under 35 U.S.C. 112. Thus, the application including claims 1 to 19 is believed to be in condition for allowance. Early and favorable action is respectfully urged.

Respectfully submitted,

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